

Appl. No. 09/751,427
Amtd. dated July 16, 2004
Reply to Office Action of April 16, 2004

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1. (cancelled)

2. (currently amended):

The device of claim 1, 26, wherein the first power management state and the second power management state each comprises a set of power management states.

3. (currently amended):

The apparatus of claim 1, 26, wherein:

the switchable first peripheral device is capable of operating as a conventional peripheral device when coupled to the bus as the slave device.

4. (currently amended):

The apparatus of claim 1, 26, wherein:

the switchable first peripheral device is capable of operating as the default bus master for the computer without assistance from the first default master, CPU.

5. (currently amended):

The apparatus of claim 4, wherein the switchable first peripheral device causes the apparatus configurable link to couple the switchable first peripheral device to the bus as the default bus master when the first default master CPU is in a the second power management state.

6. (currently amended):

The apparatus of claim 1, 26, wherein the first default master computer's CPU is in a sleeping state in the second power management state.

7. (currently amended):

The apparatus of claim 1, 26, wherein the second power management state includes power modes S3-S5 as defined in the Advanced Configuration and Power Interface (ACPI) specification.

8. (currently amended):

The apparatus of claim 1, 26, wherein the transfer rate over the configurable link bus when the switchable first peripheral device is the default bus master is different than when the first default master computer's CPU is the default bus master.

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9-14. (cancelled)

15. (currently amended):

The method of claim 14, 27, wherein the switchable first-peripheral device is capable of operating as the default bus master for the computer without assistance from the first default master CPU.

16. (currently amended):

The method of claim 15, wherein the switchable first-peripheral is capable of operating as a conventional peripheral device when coupled to the bus as the slave device.

17. (currently amended):

The method of claim 14, 27, wherein the first default master computer's CPU is in a sleeping state in the second power management state.

18. (currently amended):

The method of claim 14, 27, wherein the second power management state includes power modes S3-S5 as defined in the Advanced Configuration and Power Interface (ACPI) specification.

19. (currently amended):

The method of claim 14, 27, wherein the switchable first-peripheral device causes the configurable link to couple the switchable first-peripheral device to the bus as the default bus master when the first default master CPU is in a second power management state.

20. (cancelled)

21. (currently amended):

A system, comprising:

a sub-system to couple a plurality of slave peripheral devices to a bus;

a sub-system to couple a first default master to the plurality of slave peripheral devices through the bus;

a sub-system to detect the power management state of the first default master central processor;

a sub-system to determine whether the first default master central processor is in a first power management state or a second power management state;

a sub-system to couple the first default master central processor to the bus as a default bus master and to couple a switchable first peripheral device to the bus as a slave device if the first default master central processor is in a first power management state; and

a sub-system to couple the switchable first peripheral device to the bus as the default bus master if the first default master central processor is in a second power management state.

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22. (currently amended):

The system of claim 21, further comprising:

a sub-system to initiate a data transfer from the switchable first peripheral device if the first default master central processor is in the second power management state.

23. (currently amended):

The system of claim 21, further comprising:

a sub-system to buffer data at the switchable first peripheral device if the first default master central processor is in the second power management state.

24. (currently amended):

The system of claim 21, further comprising:

a sub-system to allow the switchable first peripheral device to directly access and communicate with a second peripheral device without assistance from the first default master central processor.

25. (currently amended):

The system of claim 21, further comprising:

a sub-system to delay the first default master central processor from transitioning from the second power management state to the first power management state.

26. (new):

An apparatus comprising:

a plurality of slave interfaces configured to couple a plurality of slave peripheral devices to a bus;

a master interface coupled to the plurality of slave interfaces, the master interface configured to couple a first default master to the plurality of slave peripheral devices through the bus; and

a switchable interface coupled to the plurality of slave interfaces and the master interface, the switchable interface configured to

couple a switchable peripheral device to the first default master through the bus as a slave device when the first default master is in a first power management state, and

couple the switchable peripheral device to the plurality of slave peripheral devices through the bus as a second default master when the first default master is a second power management state.

27. (new):

A method comprising:

coupling a plurality of slave peripheral devices to a bus;

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coupling a first default master to the plurality of slave peripheral devices through the bus;
coupling a switchable peripheral device to the first default master through the bus as a
slave device when the first default master is in a first power management state; and
coupling the switchable peripheral device to the plurality of slave peripheral devices
through the bus as a second default master when the first default master is a second
power management state.